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10/081,249	02/22/2002	Kuo-Hwa Yu	PAT-1399	6372

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Raymond Sun
12420 Woodhall Way
Tustin, CA 92782

EXAMINER	
PARK, ILWOO	

ART UNIT	PAPER NUMBER
2182	4

DATE MAILED: 10/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/081,249	YU, KUO-HWA
	Examiner	Art Unit
	Ilwoo Park	2182

-- The MAILING DATE of this communication appears on the cover sheet with th correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 February 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Pri rity under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-16 are presented for examination.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 7, 9, 11, 12, 14, and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Jolley et al., US patent No. 5,832,244.

As to claim 1, Jolley et al teach a peripheral or memory device having a bus, and a bus switching circuit that comprises:

a first bus decoder circuit coupled to the bus for decoding [col. 5, lines 1-13] signals in a first format;

a second bus decoder circuit coupled to the bus for decoding [col. 5, lines 1-13] signals in a second format;

a first bus snoop circuit [col. 6, lines 34-37] coupled to the bus;

a second bus snoop circuit [col. 6, lines 34-37] coupled to the bus;

a switch coupled to the first bus snoop circuit for receiving a first bus detect signal [col. 10, lines 60-63] therefrom, and the switch coupled to the second bus snoop circuit for receiving a second bus detect signal [col. 10, lines 63-66] therefrom; and

wherein the switch is coupled to the first bus decoder circuit for providing a first bus enable signal [col. 7, lines 17-23; col. 11, lines 1-3] thereto, and the switch is coupled to the second bus decoder circuit for providing a second bus enable signal [col. 7, lines

17-23; col. 11, lines 1-3] thereto, depending on the nature of the first and second detect signals.

4. As to claims 7 and 12, Jolley et al teach a peripheral or memory device comprising:

a bus [bus 18, 24];

a first bus decoder circuit coupled to the bus for decoding [col. 5, lines 1-13] a first type of bus signal;

a second bus decoder circuit coupled to the bus for decoding [col. 5, lines 1-13] a second type of bus signal;

means for detecting whether the bus is a first type of bus or a second type of bus, the detecting means outputting a select signal;

a switch coupled to the detecting means for receiving the select signal [col. 10, lines 60-66] therefrom; and

wherein the switch is coupled to the first bus decoder circuit for providing a first bus enable signal [col. 7, lines 17-23; col. 11, lines 1-3] thereto, and the switch is coupled to the second bus decoder circuit for providing a second bus enable signal [col. 7, lines 17-23; col. 11, lines 1-3] thereto, depending on the nature of the select signal.

5. As to claims 9 and 14, Jolley et al teach the detecting means comprises:

a first bus snoop circuit [col. 6, lines 34-37] coupled to the bus;

a second bus snoop circuit [col. 6, lines 34-37] coupled to the bus; and

wherein the switch is coupled to the first bus snoop circuit for receiving a first bus detect signal [col. 10, lines 60-63] therefrom, and the switch is coupled to the second bus snoop circuit for receiving a second bus detect signal [col. 10, lines 63-66]therefrom.

11. As to claims 11 and 16, Jolley et al teach the detecting means comprises a pin [col. 15, lines 4-22].

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 3 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jolley et al., US patent No. 5,832,244 in view of Collins, US patent No. 5,671,355.

As to claims 3 and 5, Jolley et al teach a peripheral or memory device comprising:

a bus [host bus 18, 24];

a pin [col. 15, lines 4-22]; and

a bus switching circuit that comprises:

a first bus decoder circuit coupled to the bus for decoding [col. 5, lines 1-13] signals in a first format;

a second bus decoder circuit coupled to the bus for decoding [col. 5, lines 1-13] signals in a second format;

a switch for receiving a bus select signal [type of the host bus: col. 10, lines 60-66]; and

wherein the switch is coupled to the first bus decoder circuit for providing a first bus enable signal [col. 7, lines 17-23; col. 11, lines 1-3] thereto, and the switch is coupled

to the second bus decoder circuit for providing a second bus enable signal [col. 7, lines 17-23; col. 11, lines 1-3] thereto, depending on the nature of the bus select signal.

However, Jolley et al teach do not disclose a micro-controller.

Collins teaches a peripheral or memory device, for interfacing a plurality of different types of host bus, having a micro-controller [col. 7, lines 44-47] capable of detecting the bus type of the host connected.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Jolley et al and Collins because they both teach a peripheral or memory device capable of detecting a type of a host bus connected in order to interface the plurality of different types of host bus and Collins' teaching of detecting the bus type using the micro-controller would increase flexibility in design [Collins: col. 9, lines 17-41] in contrast to hardware fixed detecting circuitry [Jolley et al: figs. 8-10].

8. Claims 10 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jolley et al as applied to claims 7 and 12 above, and further in view of Collins, US patent No. 5,671,355.

Collins teaches a peripheral or memory device, for interfacing a plurality of different types of host bus, having a micro-controller [col. 7, lines 44-47] capable of detecting the bus type of the host connected.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Jolley et al and Collins because they both teach a peripheral or memory device capable of detecting a type of a host bus connected in order to interface the plurality of different types of host bus and Collins'

teaching of detecting the bus type using the micro-controller would increase flexibility in design [Collins: col. 9, lines 17-41] in contrast to hardware fixed detecting circuitry [Jolley et al: figs. 8-10].

9. Claims 2, 8, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jolley et al as applied to claims 1, 7, and 12 above, and further in view of Chang et al., US patent No. 6,286,097.

As to claims 2, 8, and 13, Chang et al teach a bus can be either [col. 2, lines 10-14; figs. 1-2] an ISA bus or an LPC bus and an ISA bus decoder circuit and an LPC bus decoder circuit.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include an ISA bus decoder circuit and an LPC bus decoder circuit into the plurality of Jolley et al's bus decoder circuits in order to increase adaptability for a bus connection [Chang et al: col. 2, lines 10-14].

10. Claims 4 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jolley et al and Collins as applied to claims 3 and 5 above, and further in view of Chang et al., US patent No. 6,286,097.

As to claims 4 and 6, Chang et al teach a bus can be either [col. 2, lines 10-14; figs. 1-2] an ISA bus or an LPC bus and an ISA bus decoder circuit and an LPC bus decoder circuit.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include an ISA bus decoder circuit and an LPC bus decoder

circuit into the plurality of Jolley et al and Collins' bus decoder circuits in order to increase adaptability for a bus connection [Chang et al: col. 2, lines 10-14].

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ilwoo Park whose telephone number is (703) 308-7811. The examiner can normally be reached on Monday through Friday from 9:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey A Gaffin can be reached on (703) 308-3301. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA, 4th Floor (Receptionist).

Ilwoo Park

September 26, 2003